Chapter 8
Parallel Connections

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This chapter explains the factors that inhibit current sharing and the notes when IGBT is connected in parallel.

When connecting IGBT modules in parallel, it is necessary to properly manage the elements' characteristics.
Otherwise, a current sharing imbalance may occur depend on the characteristics distribution between the parallel connected modules.
The parallel connection techniques are introduced in this chapter using 1in1 and 2in1 module shown in Table 1-1. If 6in1 and PIM(7in1) module are used parallel connection, please contact of technical confirmation to Fuji Electric Device Technology.

1 Factors that inhibit current sharing

1.1 On-state current imbalance

An on-state current imbalance may be caused by the following two factors:

(1) $V_{CE(sat)}$ distribution
(2) Main circuit wiring resistance distribution

1) Current imbalance caused by $V_{CE(sat)}$ distribution

As shown in Fig. 8-1, a difference in the output characteristics of two IGBT modules connected in parallel can cause a current imbalance.
The output characteristics of Q_1 and Q_2 shown in Fig. 8-1, can be approximated as follows:

$$V_{CEQ1} = V_{01} + r_1 \times I_{C1}$$

$$r_1 = V_1 / (I_{C1} - I_{C2})$$

$$V_{CEQ2} = V_{02} + r_2 \times I_{C2}$$

$$r_2 = V_2 / (I_{C1} - I_{C2})$$

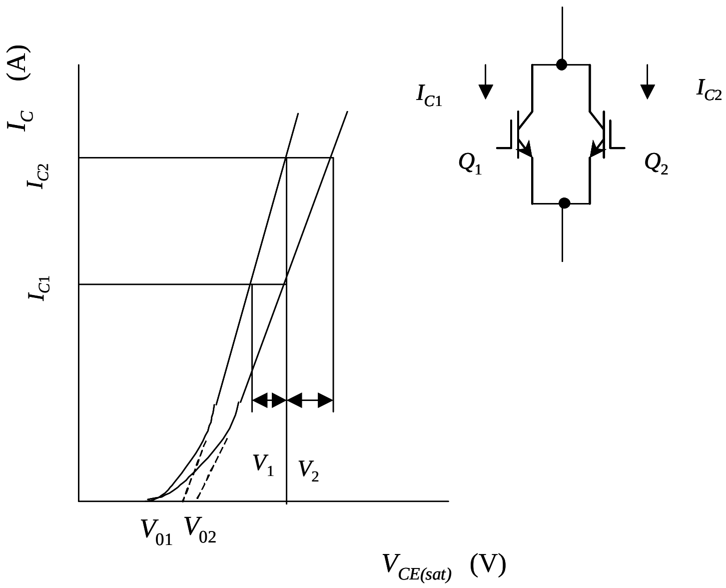

Fig. 8-1 Example of a $V_{CE(sat)}$ pair

Based on the above, if the I_{Ctotal} (=I_{C1}+I_{C2}) collector current is made to flow through the circuit of Q_1 and Q_2 connected in parallel, then the IGBT's collector current becomes the following:

$$I_{C1} = (V_{02} - V_{01} + r_2 \times I_{Ctotal})/(r_1 + r_2)$$
$$I_{C2} = (V_{01} - V_{02} + r_1 \times I_{Ctotal})/(r_1 + r_2)$$

$V_{CE(sat)}$ becomes a major factor in causing current imbalances. Therefore, in order to ensure the desired current sharing it is necessary to pair modules that have a similar $V_{CE(sat)}$.

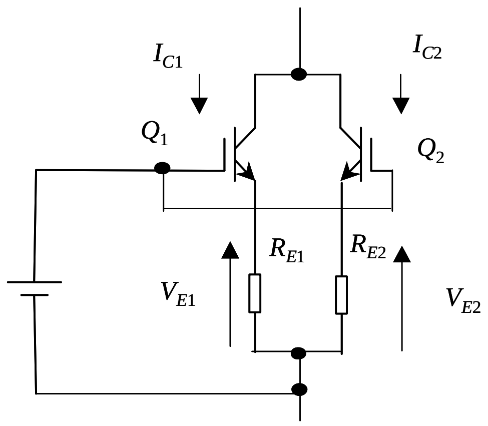

Fig. 8-2 The effect of main circuit wiring resistance

2) Main circuit wiring resistance distribution

The effect exerted on current sharing by the main circuit's wiring resistance can be seen in Fig. 8-2. The effect is larger with emitter resistance than with collector resistance, so collector resistance has been omitted here. If there is resistance in the main circuit, then the parity of the slope of the IGBT modules' output characteristics will lessen, and the collector current will drop. So, depending on how well the collector current can flow through this resistance, an electrical potential difference may appear,

the actual gate-emitter voltage drop (V_{GE}=V – VE), the IGBTs' output characteristics change and the collector current decline. Therefore, if $R_{E1}>R_{E2}$, then the slope of the Q_1 output characteristics will lessen and if $I_{C1}<I_{C2}$ then a current sharing imbalance will appear.
In order to reduce this imbalance, it is necessary to make the wiring on the emitter side as short and as uniform as possible.

1.2 Factors of current imbalances at turn-on and turn-off

The factors of current imbalances at turn-on and turn-off can be divided into module characteristics distribution and main circuit wiring inductance distribution.

1) Module Characteristics distribution

An IGBTs' switching current imbalance is mostly determined by an on-state current imbalance, therefore if the on-state current imbalance is controlled simultaneously, so will the switching voltage imbalance.

2) Main circuit wiring inductance distribution

Since the previously explained effect of resistance on current sharing is much the same as that of inductance on current sharing, inductance can be substituted for resistance in Fig. 8-2. As the collector current changes very suddenly during IGBT switching, a voltage is generated at both ends of inductance. The polarity of this voltage tends to hamper switching, so the switching time will increase. Therefore, if inductance is not controlled, then switching time will be delayed and the current will be concentrated into one of the modules. In order to reduce this imbalance, it is necessary to make the wiring on the emitter side as short and as uniform as possible.

2 Parallel connections

2.1 Wiring

The ideal parallel connection wiring is "both uniform and short", but when seen from the point of view of equipment mass production, it is often to implement this fully. Therefore, it is necessary to design a layout as close to the ideal as possible. For this purpose, several basic points of caution are illustrated below.

1) Drive circuit wiring

When connecting IGBT modules in parallel, due to the gate circuit's wiring inductance and the IGBT's input capacitance, as the gate voltage rises a parasitic oscillation may occur. Therefore, in order to prevent this oscillation, a gate resistor should be series wired to each of the modules gates. (As illustrated in Fig. 8-3)
As stated previously, if the drive circuit's emitter wiring is connected in a different position from the main circuit, then the modules' transient current sharing (especially at turn-on) will become imbalanced. However, IGBT modules have an auxiliary emitter terminal for use by drive circuits. By using this terminal, the drive wiring of each module becomes uniform, and transient current imbalances attribute to drive circuit wiring can be controlled.
Furthermore, be sure to lead the wiring out from the center of the modules parallel connection, tightly wind it together, and lay it out so that it is as far away from the main circuit as possible in order to avoid mutual induction.

2) Main circuit wiring

As stated previously, if the resistance or the inductance of the main circuit is not uniform, then the current sharing of the modules connected in parallel will be unbalanced.
Furthermore, if the inductance of the main circuit is large, then the surge voltage at IGBT turn-off will also be high (for details, refer to Chapter 5, "Protection Circuit Design", of this manual). Therefore, for the purpose of reducing wiring induction and maintaining the temperature balance of each module, consider setting the modules that are to be connected in parallel as close together as possible and making the wiring as uniform as possible.
Also, take out the collector and emitter lead wires from the center of the parallel connection, and, in order to avoid mutual induction, do not wire them in parallel.

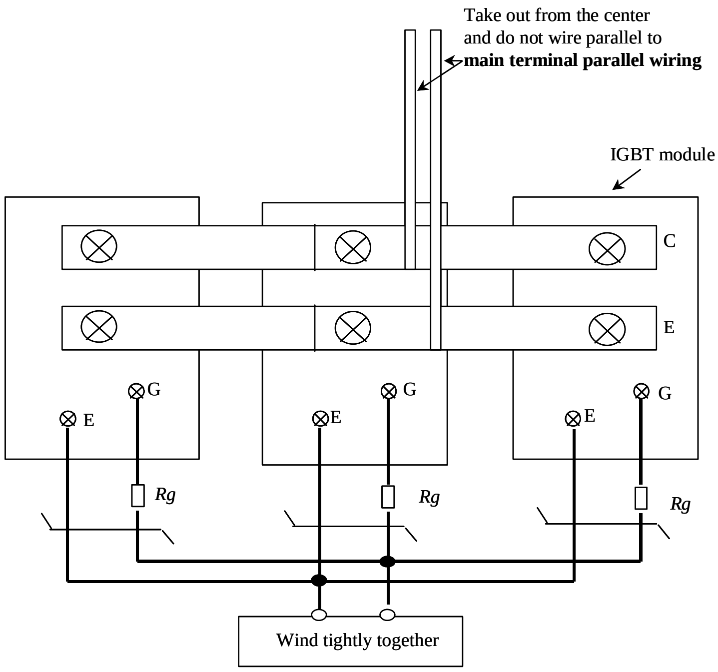

Fig. 8-3 Example of parallel connection layout

2.2 Relationship of module characteristics to current sharing

As stated previously, from among a module's individual characteristics, the $V_{CE(sat)}$ distribution has a strong effect on current sharing.
When n-number of modules are connected in parallel, the following shows the maximum current that can be applied under the worst case conditions where the entire current is concentrated into one module:

$$\sum I = I_{C(\max)}\left[1+(n-1)\frac{\left(1-\frac{\alpha}{100}\right)}{\left(1+\frac{\alpha}{100}\right)}\right]$$

$$\alpha = \left[\frac{I_{C1}}{I_{C(ave)}}-1\right]\times 100$$

Here $I_{C(max)}$ represents the maximum current for a single element that the modules rated RBSOA and power dissipation loss will allow. It is especially important to pay attention to power dissipation loss, because this changes depending on the operating conditions (switching frequency, drive conditions, heat dissipation, snubber conditions, etc.). For details on power dissipation loss, refer to Chapter 6, "Cooling Design", of this manual. For example, if α=16%, $I_{C(max)}$=200A and n=4, then ΣI=634.4A, and the parallel connected total current should be set so as not to exceed this value. It is important not to make the error of simply calculatingΣI=200×4=800A.

Fig. 8-4 shows the difference of VCE(sat) and the current imbalance proportion in parallel connections. Because the temperature coefficient of the output characteristic is a positive characteristic as shown in Fig. 8-5, the current imbalance proportion α becomes small U-series IGBT compared with N-series IGBT.

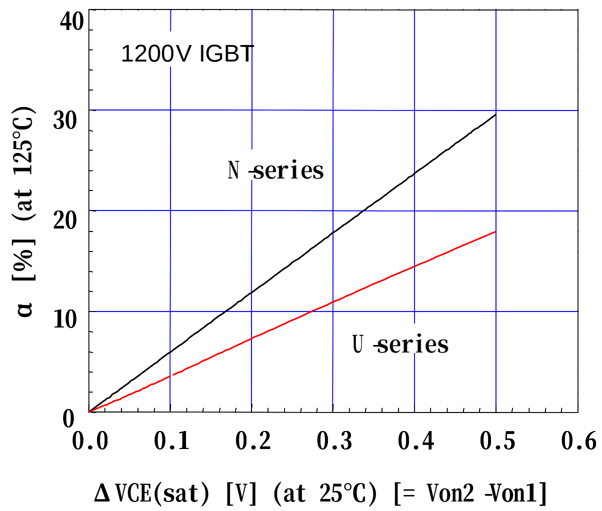

Fig. 8-4 Current imbalance proportion in parallel connections

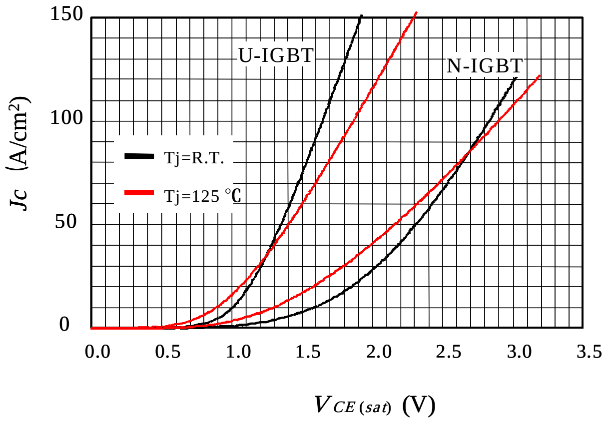

Fig. 8-5 Comparison of $V_{CE(sat)}$-Jc characteristics

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